PVP 14

Code: CS4T5

II B.Tech - II Semester–Regular / Supplementary Examinations
April 2019

COMPUTER ORGANIZATION
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks
11 x 2 = 22 M

1.

a) What is the function of a T flip-flop?
b) What are called don't care conditions?
c) State the significance of PSW (Program Status Word).
d) How effective address is computed in indexed addressing mode?
e) What is a priority interrupt?
f) Define an interface.
g) Briefly explain about write-through cache update mechanism.
h) Mention different types of semiconductor memories
i) What is a hardware lock mechanism?
j) What is a semaphore?
k) Define virtual memory concept.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.
3 x 16 = 48 M

2. a) Explain the flip-flop excitation tables for JK flip-flop. 8 M

   b) Simplify the following expression in product-of-sums form. x'z'+y'z'+yz'+xy. 8 M

3. a) Explain the operation of a memory stack. 8 M

   b) Illustrate the instruction formats. 8 M

4. a) Explain about strobe control method of Asynchronous Data transfer. 8 M

   b) How polling is used for establishing the priority of simultaneous interrupts. 8 M

5. a) Explain about the mapping procedures adopted in the organization of cache memory. 8 M

   b) Discuss about LRU and FIFO page replacement algorithms. 8 M

6. a) Explain about inter process synchronization. 8 M

b) Discuss few bus arbitration procedures that use dynamic algorithms. 8 M